EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	0	(((select$3 configur$5) adj signal) with (error adj (bit flag signal)) with ((select$3 configur$5) adj signal) with ((adjacent previous) near2 (row column))).clm.	US-PGPUB	OR	ON	2007/02/28 13:47

Interference Seach History Report

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	0	(((select$3 configur$5) adj signal) with (error adj (bit flag signal)) with ((select$3 configur$5) adj signal) with ((adjacent previous) near2 (row column))).clm.	US-PGPUB	OR	ON	2007/02/28 13:47
L2	13	L1 and PLD and "configuration controller"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 13:42
S48	12	S47 and PLD and "configuration controller"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 13:36
L3	332	(FPGA PLD) and (configuration adj (controller processor))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 13:36
L1	16333	(714/2,710,711,715,718-720,733 365/200,201 326/10,38,39,41).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/28 13:36
S56	32	(select$3 with error with adjacent with column)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:36
S50	0	S49 and (select$3 with error with adjacent with column)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:36
S55	2	("20040250181").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:12

EAST Search History

S54	0	US20040250181	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:12
S53	19	09/343,344	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:12
S52	19	09/343344	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:01
S51	27	("20040136319"|"20050022065"|"20030037278"|"20040068682"|"20040073829"|"5991891"|"6128750"|"6316980"|"6317352"|"6389494"|"6502161"|"6505305"|"6571355").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 16:01
S49	332	(FPGA PLD) and (configuration adj (controller processor))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 13:53
S43	270	(FPGA PLD) and (configuration adj (controller processor))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/27 13:53
S40	55	PLD and "configuration controller"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 12:41
S47	15774	(714/2,710,711,715,718-720,733 365/200,201 326/10,38,39,41).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 12:34

EAST Search History

S41	15134	(714/2,710,711,715,718-720,733 365/200,201 326/10,38,39,41).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 12:34
S46	1	(FPGA PLD) and (configuration adj (controller processor)) and BIST	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 14:21
S45	12	S44 not S42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 14:16
S44	23	S43 and S41	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 14:16
S42	11	S40 and S41	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 14:08
S35	15134	(714/2,710,711,715,718-720,733 365/200,201 326/10,38,39,41).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/26 14:07
S39	52	S35 and S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:26
S38	171	(concurrent$2 simultaneous$2) near4 (BIST self-test)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:25

EAST Search History

S37	109	S36 and (BIST self-test)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:25
S36	1074	S35 and (defect$3 near3 column) and ((redundant spare) near2 column)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:23
S25	11217	(714/710,711,715,718-720,733 365/200,201).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 16:21
S34	2	(configuration near2 control$3) and ((BIST "built in self test" "built-in self-test" self-test "self test") near2 control$3) and (("random access memory" RAM SRAM "volatile memory") same (redundant near3 column))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:42
S33	2	(configuration near2 control$3) and ((BIST "built in self test" "built-in self-test" self-test "self test") near2 control$3) and ("random access memory" RAM SRAM "volatile memory") same (redundant near3 column)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:42
S32	117	(configuration near2 control$3) and ((BIST "built in self test" "built-in self-test" self-test "self test") near2 control$3) and ("random access memory" RAM SRAM "volatile memory")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:41
S31	0	S29 and (self-test "self test")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:37
S30	31	"L10" and (self-test "self test")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:35

EAST Search History

S29	10	S25 and ((FPGA PLD PLA) same (RAM memory)) and (redundan$2 (column row)) and ((program$4 configur$5) near4 (volatile near2 memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:33
S28	176	S25 and ((FPGA PLD PLA) same (RAM memory)) and (redundan$2 (column row))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:10
S26	234	S25 and ((FPGA PLD PLA) same (RAM memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:09
S27	1	S25 and S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:07
S24	0	S22 not S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:06
S23	6	((FPGA PLD PLA) same (RAM memory)) and ((BIST self-test) same (BISR self-repair))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:06
S22	6	((FPGA PLD PLA) same (RAM memory)) and ((BIST self-test$3) same (BISR self-repair$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:05
S20	6	((FPGA PLD PLA) same (RAM memory)) and ((BIST self-test) same (BISR self-repair))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/25 10:05

EAST Search History

S21	5	S20 not S19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 18:34
S19	1	((FPGA PLD PLA) with (RAM memory)) and ((BIST self-test) same (BISR self-repair))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 18:34
S18	1	((FPGA PLD PLA) with ((RAM memory) near2 array)) and ((BIST self-test) same (BISR self-repair))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 18:34
S17	0	((FPGA PLD PLA) with ((RAM memory) near2 array)) same ((BIST self-test) same (BISR self-repair))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 18:32
S15	1	configur$3 with (FPGA PLD "programmable logic device" "programmable logic") and (BIST self-test) and ((redundan$2 repairable) near3 (memory column))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 18:09
S16	9	(program$4 configur$3) with (FPGA PLD "programmable logic device" "programmable logic") and (BIST self-test) and ((redundan$2 repairable) near3 (memory column))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:49
S14	1	configur$3 with (FPGA PLD "programmable logic device" "programmable logic") and (BIST self-test) and (redundan$2 near3 (memory column))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:30
S13	179	configur$3 with (FPGA PLD "programmable logic device" "programmable logic") and (BIST self-test)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:28

EAST Search History

S12	5154	configur$3 with (FPGA PLD "programmable logic device" "programmable logic")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:27
S9	26	(FPGA PLD "programmable logic device" "programmable logic") and $2RAM and (redundan$2 near3 column) and (BIST self-test)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 16:25
S11	0	S9 and ((setting stor$3) near3 error)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:37
S10	0	(FPGA PLD "programmable logic device" "programmable logic") and $2RAM and (redundan$2 near3 column) and (BIST self-test) and ((setting stor$3) near3 error near2 flag)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:37
S5	29	S2 and (FPGA PLD "programmable logic device" "programmable logic" "programmable memory")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:31
S8	15	S7 and (redundan$2 repair$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:01
S7	26	S5 not S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 15:01
S6	3	S5 and BIST	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:55

EAST Search History

S2	41	("3995261"|"4020469"|"4700187"|"4899067"|"5153880"|"5255227"|"5459342"|"5485102"|"5498975"|"5513144"|"5592102"|"5742556"|"5764577"|"5777887"|"5889413"|"5914616"|"6166559"|"6167558"|"6344755"|"6356514"|"6560740").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:54
S4	5	09/924365 and Ling	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:43
S3	5	09/924365	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:43
S1	39	("3995261"|"4020469"|"4700187"|"4899067"|"5153880"|"5255227"|"5459342"|"5485102"|"5498975"|"5513144"|"5592102"|"5742556"|"5764577"|"5777887"|"5889413"|"5914616"|"6166559"|"6167558"|"6344755"|"6356514").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/04/24 14:42